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In re Patent Application of:
CASSAGNES
Serial No. **10/039,233**
Filing Date: **December 31, 2001**

REMARKS

The Examiner is thanked for the thorough examination of the present application, and for correctly indicating the allowability of the subject matter of Claims 17, 21, 28, and 34. Independent Claims 13, 23, and 30 have been amended to include the subject matter of their respective dependent Claims 14, 25, and 31, which have been canceled. Claim 15 has also been canceled.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a decoding circuit for decoding a biphase signal having a pair of states. As recited in amended independent Claim 13, for example, the decoding circuit includes a precharging register for precharging the states of the biphase signal, where one state of the pair of states is precharged at each pulse of a periodic precharging signal. The decoding circuit further includes a verification circuit for comparing the two states of the pair of states to detect an error. The verification circuit provides an error signal based upon detecting the error, wherein the error comprises the two states being equal.

Independent Claims 19 and 23 are directed to related circuits, and independent Claim 30 is directed to a related method. Each of these claims recites that the error comprises the two states being equal, similar to Claim 13.

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II. The Claims Are Patentable

The Examiner rejected independent Claims 13, 19, 23, and 30 (as well as dependent Claims 14, 25, and 31) over Hiramatsu (U.S. Patent No. 5,778,031). This patent is directed to a circuit for decoding bi-phase signals included in an audio signal. Referring to FIG. 5 of Hiramatsu, the circuit includes a shift register 31 for storing three successive states ai, ai+1, ai+2 (see col. 1, lines 62-63), circuits 32-44 for comparing the state ai with ai+1 and the state ai+1 with ai+2, and deducing states to be paired, i.e., (ai, ai+1) or (ai+1, ai+2). A carrier extracting circuit 50 extracts the bi-phase signal from the audio signal (see col. 5, lines 15-20), and decoding circuitry (components 6-12) decodes the bi-phase signal (see col. 5, lines 22-36).

The Examiner contends that Hiramatsu teaches comparing two states of a pair of states of a bi-phase signal to detect an error (i.e., when the two states are equal), and providing an error signal based upon detecting the error. As support, the Examiner cites col. 5, lines 57-62, and col. 7, line 23 of Hiramatsu. It is respectfully submitted that the Examiner mischaracterizes Hiramatsu, as this reference does not teach that detecting two states being equal constitutes an error as recited in the above-noted independent claims.

In particular, in Hiramatsu the circuit 3a including the elements 32-44 is a pair determining circuit (see col. 4, lines 43-46), which is also referred to in the patent as a

"malfunction-preventing means." The first function of this circuit is to determine which states are to be paired, i.e., ai and ai+1 or ai+1 and ai+2. If ai and ai+1 are the same, and ai+1 and ai+2 differ from each other, then ai+1 and ai+2 are paired. If ai and ai+1 differ from each other, and ai+1 and ai+2 are the same, then ai and ai+1 are to be paired. This is due to the fact that the bi-phase signal represents "1" by "10" and "0" by "01."

A second function of this circuit is to detect an error, for example if the 3 states are "ai,ai+1,ai+2" = "010". In this case, ai and ai+1 are different, and ai+1 and ai+2 are also different, so it is not possible to determine which states are to be paired. See, e.g., col. 6, lines 41-48, which is reproduced below for the Examiner's convenience:

> "Further, if 3 bits of data assumes "010" and the outputs from logic operation circuit 40 are X=0 and Y=0 by some cause, updown counter 41 neither counts up nor counts down. However, as long as the count value is larger than the prescribed threshold value α1=1 of the first comparator 42, the circuit determines that there is error in the three bits of data, and continues to determine the pairs as (a0, a1), (a2, a3), (a4, a5) … , similar to the aforementioned example."

Thus, in the circuit of Hiramatsu, two comparisons are necessary to detect an eventual error, namely ai with ai+1 and ai+1 with ai+2. An error signal is provided only if it is not possible to determine which states should be paired, i.e., if ai does not equal ai+1 and ai+1 does not equal ai+2. In sharp

contrast, the above-noted independent claims recite that an error signal is provided when the two states of the pair of states are equal. Therefore, not only does Hiramatsu not teach all of the recitations of the above-noted claims, it teaches away from the claimed combination.

Accordingly, it is submitted that independent Claims 13, 19, 23, and 30 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner of Patents on this 3 day of August, 2005.